64-Position Up/Down Control Digital Potentiometer

Preliminary Technical Data

AD5227

FEATURES

- **64-Position**
- **10k, 50k, 100kΩ end-to-end terminal resistance**
- **Simple Up/Down Digital or Manual Configurable Control**
- **Mid-Scale Preset**
- **Low Potentiometer Mode TC 10ppm/°C**
- **Low Rheostat Mode TC 35ppm/°C**
- **Ultra low power, I_{DD} = 5μA Max**
- **Fast Adjustment Time, ts = 1μs**
- **Chip Select Enable Multi-Devices Operation**
- **Low Operating Voltage, 2.7V to 5.5V**
- **Automotive Temperature Range -40°C to +105°C**
- **Compact Thin SOT23-8 (2.9 mm × 3 mm) package**

APPLICATIONS

- **Mechanical Potentiometers and Trimmers Replacements**
- **LCD Contrast, Brightness, and Backlight Controls**
- **Portable Electronics Level Adjustments**
- **Programmable Power Supply**
- **Digital Trimmers Replacements**
- **Automatic Close Loop Control**

GENERAL DESCRIPTIONS

AD5227 is Analog Devices latest 64-Step Up/Down Control Digital Potentiometer[1]. This device performs the same electronic adjustment function as a 5V potentiometer or variable resistor. Its common 3-wire up/down interface allows high-speed as well as low-speed digital controls. AD5227 presets to mid-scale in power up. When $\overline{CS}$ is enabled, the Up/Down direction is depended on the state of U/$\overline{D}$ and it executes at every clock pulse. The interface is simple that can be controlled by any host controllers, discrete logics, and manually with rotary encoder or push buttons. AD5227 adequate resolution, small footprint, and simple interface enable it to be the potential replacements of mechanical potentiometers and trimmers with typically 6X improved resolution, solid-state reliability, and design layout flexibility. These enhancements can result in considerable cost saving in end users' systems.
The AD5227 is available in compact thin SOT23-8 package. All parts are guaranteed to operate over the extended industrial temperature range of -40°C to +105°C.

For users who consider EEMEM potentiometers, they may refer to some recommendations in the Applications Section.

FUNCTIONAL BLOCK DIAGRAM

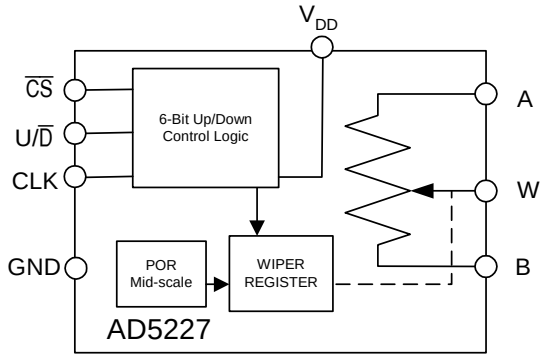
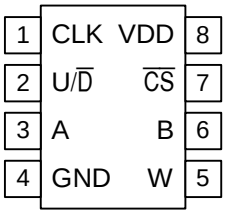


Figure 1. Functional Block Diagram

Table 1. Truth Table

$\overline{CS}$	CLK	U/$\overline{D}$	Operation
0	↓	0	R_{WB} Decrement, R_{WA} Increment
0	↓	1	R_{WB} Increment, R_{WA} Decrement
1	X	X	No Operation

PIN CONFIGURATION



SOT23-8

Figure 2. Pin Configuration

Note
1. The term digital potentiometer and RDAC are used interchangeably.

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REVISION HISTORY

Revision PrD: Initial Version

Table 2. ELECTRICAL CHARACTERISTICS 10k , 50k, 100kΩ VERSION (V_{DD} = +3V±10% or +5V±10%, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +105°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A=NC	-1	±0.25	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A=NC	-1	±0.5	+1	LSB
Nominal resistor tolerance	$\Delta R_{AB}/R_{AB}$	T_A = 25°C	-30		30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$				35	ppm/°C
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 5V		120	200	Ω
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 2.7V		200	400	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Resolution	N				6	Bits
Integral Nonlinearity[4]	INL		–1	±0.5	+1	LSB
Differential Nonlinearity[4]	DNL		–1	±0.1	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Mid-scale		5		ppm/°C
Full-Scale Error	V_{WFSE}	+32 Steps from Mid-scale (Full-scale)	–2	-0.5	+0	LSB
Zero-Scale Error	V_{WZSE}	-32 Steps from Mid-scale (Zero-scale)	0	+0.5	+1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		0		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Mid-scale		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Mid-scale		60		pF
Common Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = +5V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = +5V			0.8	V
Input Current	I_{IL}	V_{IN} = 0V or +5V			1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		+2.7		+5.5	V
Supply Current	I_{DD}	V_{IH} = +5V or V_{IL} = 0V, V_{DD} = +5V			5	µA
Power Dissipation[10]	P_{DISS}	V_{IH} = +5V or V_{IL} = 0V, V_{DD} = +5V			25	µW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5V ±10%		0.05	0.15	%/%
DYNAMIC CHARACTERISTICS[6,9,11]						
Bandwidth –3dB	BW	R_{AB} = 10k/50k/100kΩ, Mid-scale		600/X/Y		kHz
Total Harmonic Distortion	THD_W	V_A =1Vrms + 2V dc, V_B = 2V DC, f=1KHz		0.05		%
V_W Settling Time	t_S	V_A= V_{DD}, V_B=0V, ±1 LSB error band		1		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5KΩ, f = 1kHz		14		nV√Hz
INTERFACE TIMING CHARACTERISTICS applies to all parts(Notes 6,12)						
Input Clock Pulse Width	t_{CH},t_{CL}	Clock level high or low	10			ns
$\overline{CS}$ to CLK Setup Time	t_{CSS}		10			ns
$\overline{CS}$ Rise to CLK Hold Time	t_{CSH}		10			ns
U/$\overline{D}$ to Clock Fall Setup Time	t_{UDS}		10			ns

NOTES:

1. Typicals represent average readings at +25°C, V_{DD} = +5V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
4. INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0V. DNL specification limits of ±1LSB maximum are Guaranteed Monotonic operating conditions.
5. Resistor terminals A,B,W have no limitations on polarity with respect to each other.
6. Guaranteed by design and not subject to production test.
7. Measured at the A terminal. The A terminal is open circuited in shutdown mode.
9. Bandwidth, noise and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value result in the minimum overall power consumption.
10. P_{DISS} is calculated from (I_{DD} x V_{DD}). CMOS logic level inputs result in minimum power dissipation.

11. All dynamic characteristics use V_{DD} = +5V.
12. See timing diagram for location of measured values. All input control voltages are specified with t_R=t_F=1ns(10% to 90% of V_{DD}) and timed from a voltage level of 1.6V. Switching characteristics are measured using both V_{DD} = +5V.

Absolute Maximum Ratings

Table 3. AD5227 Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	–0.3, +7V
V_A, V_B, V_W to GND	GND, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20mA
I_{WB} Continuous (R_{WB} ≤ 1 kΩ, A open) [1]	±5mA
I_{WA} Continuous (R_{WA} ≤ 1 kΩ, B open) [1]	±5mA
Digital Input Voltage to GND	0V, V_{DD}
Operating Temperature Range	–40°C to +105°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 – 30 sec)	245°C
Thermal Resistance[2] θ_{JA},	230°C/W

[1]Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package. V_{DD} = 5 V.
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Package Power Dissipation = (T_JMAX – T_A) / θ_{JA}

Pin Configurations And Functional Descriptions

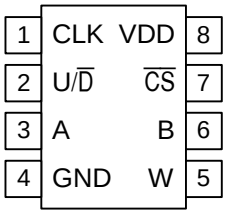

Figure 3. SOT23-8

Table 4. Pin Function Descriptions

Pin No.	Name	Description
1	CLK	Clock Input. Each Clock Pulse Executes The Step-Up or Step-Down of the Resistances. The Direction is Determined By The State in U/$\overline{D}$ Pin. Clock is Negative Edge Trigger
2	U/$\overline{D}$	Up/Down Selections. Logic 1 Selects Up and 0 Selects Down
3	A	Resistor Terminal A. GND≤V_A≤V_{DD}
4	GND	Common Ground
5	W	Wiper Terminal W. GND≤V_W≤V_{DD}
6	B	Resistor Terminal B. GND≤V_B≤V_{DD}
7	$\overline{CS}$	Chip Select. Active Low
8	V_{DD}	Positive Power Supply, +2.7 V to +5.5 V

INTERFACE TIMING DIAGRAM

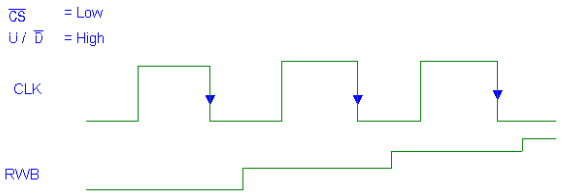

Figure 4.Stepping Up R_{WB}

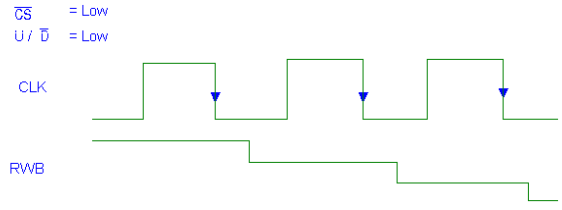

Figure 5. Stepping Down R_{WB}

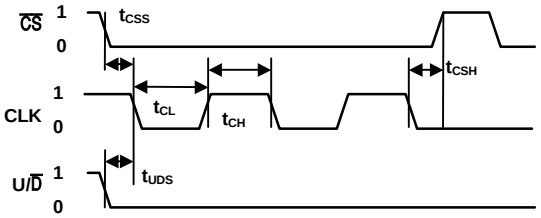

Figure 6. Detail Timing Diagram

OPERATION

The AD5227 provides a 64 position digitally-controlled potentiometer device. It presets to a mid-scale at system power ON. When $\overline{CS}$ is enabled, changing the resistance settings is achieved by clocking the CLK pin. The direction of stepping is controlled by the U/$\overline{D}$ control input. Additional CLK pulses will not change the wiper setting when the wiper hits the maximum or the minimum setting. When push button switch is used to control the clock, appropriate de-bounce circuitry should be considered. The timing requirements are shown in Figure 6.

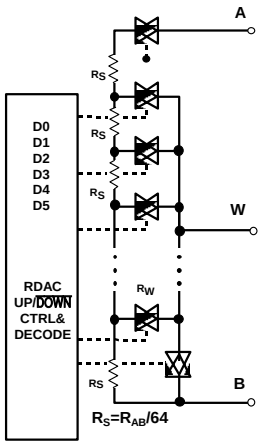

Figure 7. AD5227 Equivalent RDAC Circuit

PROGRAMMING THE DIGITAL POTENTIOMETERS

Rheostat Operation

If only the W-to-B or W-to-A terminals are used as variable resistor, the unused terminal can be opened or shorted with W, such operation is called rheostat mode, Figure 8.

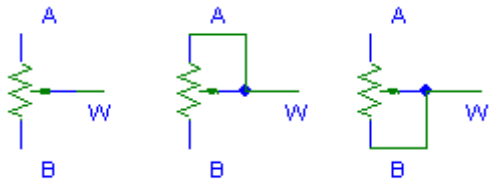

Figure 8. Rheostat Mode Configuration

The end-to-end resistance R_{AB} has 64 contact points accessed by the wiper terminal, plus the B terminal contact if R_{WB} is used, , see Figure 7. Clocking the CLK input will step R_{WB} by one step and the direction is determined by the state of U/$\overline{D}$ pin. In the open loop applications, the change of resistance, R_{WB} can be determined by the number of clock pulses applied to the clock pin provided its maximum and minimum settings are not reached. The R_{WB} can therefore be approximated as

$$\Delta R_{WB} = \pm\left(CP \cdot \frac{R_{AB}}{64} + R_W \right) \quad (1)$$

where:
CP is the number of clock pulses.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on-resistance of the internal switch.

Since in the lowest end of the resistor string, a finite wiper resistance of 60 is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, the B-terminal can be opened or shorted to W. The R_{WA} can also be approximated if its maximum and minimum settings are not reached.

$$\Delta R_{WA} = \pm\left((64 - CP) \frac{R_{AB}}{64} + R_W \right) \quad (2)$$

Equations 1 and 2 do not apply when CP = 0.

The typical distribution of the resistance tolerance from device to device is process lot dependent and is possible to have ±30% tolerance.

Potentiometer Mode Operation

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation, Figure 9.

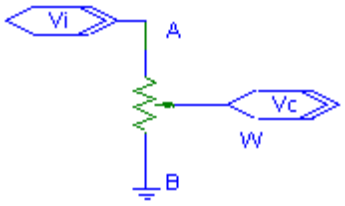

Figure 9. Potentiometer Mode Configuration

The transfer function is:

$$\Delta V_W = \frac{\frac{CP}{64}R_{AB} + R_W}{R_{AB} + 2R_W}V_A \qquad (3)$$

If we ignore the effect of the wiper resistance, the transfer function simplifies to

$$\Delta V_W = \frac{CP}{64}V_A \qquad (4)$$

Unlike in rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratio-metric function of CP/64 with a relatively small error contributed by the R_W terms, the tolerance effect is therefore almost cancelled. Although the thin film step resistor R_S and CMOS switches resistance R_W have very different temperature coefficients, the ratio-metric adjustment also makes the overall temperature coefficient effect reduced to 5ppm/°C except at low value codes where R_W dominates.

Potentiometer mode operations include others operations such as opamp input and feedback resistors network and other voltage scaling applications. A, W, and B terminals can in fact be input or output terminals and have no polarity constraint provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed VDD-to-GND.

INTERFACING

The AD5227 contains a three-wire serial input interface. The three inputs are clock (CLK), $\overline{CS}$ (Chip Select), and up/down control (U/$\overline{D}$). These inputs can be controlled digitally for optimum speed and flexibility. Standard logic families work well. On the other hand, they can also be controlled by mechanical means for simple manual operation. The states of the $\overline{CS}$ and U/$\overline{D}$ can be selected by the mechanical switches. The CLK input can be controlled by a pushbutton but it should be properly debounced by flip-flops or other suitable means. The negative-edge sensitive CLK input requires clean transitions to avoid clocking multiple pulses into the internal UP/Down counter register.

When $\overline{CS}$ is pulled low, a clock pulse increments or decrements the up/down counter and the direction is determined by the state of the U/$\overline{D}$ control pin. When the state of U/$\overline{D}$ remains, the device continues to change to the same direction under consecutive clocks until it hits the end of the resistance setting.

All digital inputs are protected with a series input resistor and parallel Zener ESD structure shown in Figure 10. Applies to digital input pins $\overline{CS}$, U/$\overline{D}$, and CLK.

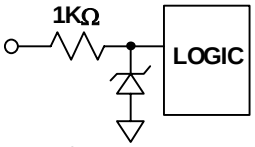

Figure 10. Equivalent ESD Protection Digital Pins

Terminal Voltage Operation Range

The AD5227 is designed with internal ESD diodes for protection but they also set the boundary of the terminal operating voltages. Positive signals present on terminal A, B, or W that exceeds V_{DD} will be clamped by the forward biased diode. There is no polarity constraint between V_{AB}, V_{WA}, and V_{WB} but they cannot be higher than V_{DD}-to-GND.

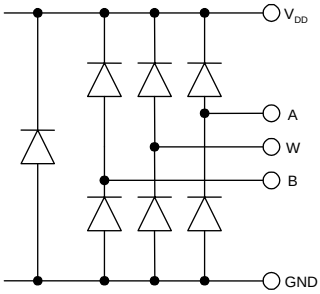

Figure 11. Maximum Terminal Voltages Set by V_{DD} and GND

Power-Up and Power-Down Sequences

Since there are ESD protection diodes that limit the voltage compliance at terminals A, B, and W (Figure 11), it is important to power V_{DD} before applying any voltage to terminals A, B, and W. Otherwise, the diodes will be forward biased such that V_{DD} will be powered unintentionally and may affect the rest of the users' circuit. Similarly, V_{DD} should be powered down last. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}.

Layout and Power Supply Biasing

It is always a good practice to employ compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors. Low ESR (Equivalent Series Resistance) 1µF to 10µF tantalum or electrolytic capacitors should be applied at the

supplies to minimize any transient disturbance and filter low frequency ripple. Figure 12 illustrates the basic supply-bypassing configuration for the AD5227

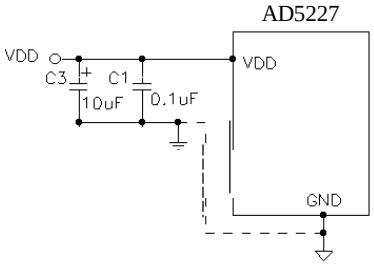

Figure 12. Power Supply Bypassing

The ground pin of the AD5227 is a digital ground reference. To minimize the digital ground bounce, the AD5227 ground terminal should be joined remotely to the common ground ground, Figure 12

APPLICATIONS

Manual Control with Push Button and Toggle Switch

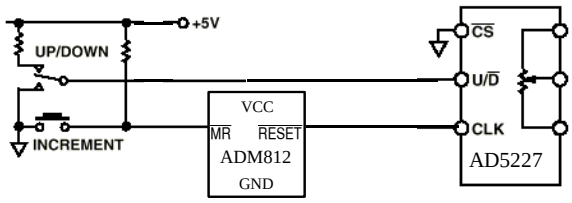

Figure 13. Manual Push Button Up/Down Control

Manual Control with Rotary Encorder

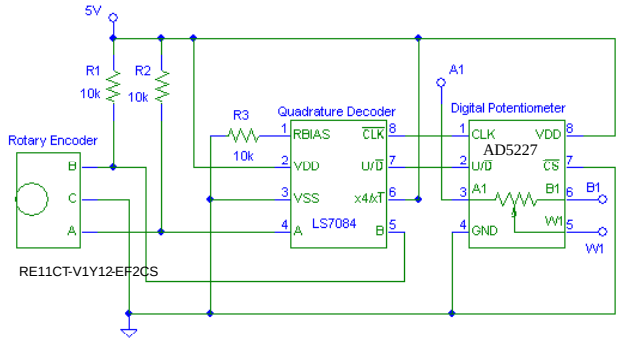

Figure 14. Manual Rotary Control

Simple Automatic Controller

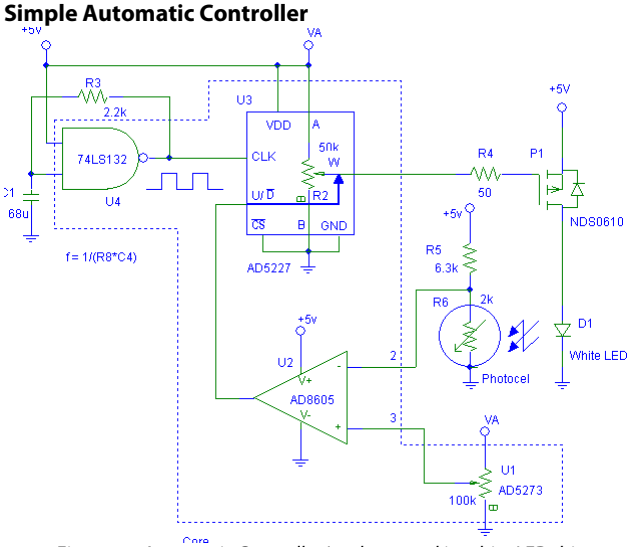

Figure 15. Automatic Controller Implemented in white LED driver

Figure 15 shows a simple automatic close loop controller that can be used in many different applications. The core of the controller consists of a one time programmable digital pot, a comparator, a 6-bit up/down control digital pot, and a Schmitt trigger NAND gate. For illustration purpose, the application shows a conceptual linear control of white LED. Typical white LEDs employ PWM controls for efficiency purpose but the circuit above can be expanded to PWM with an addition of a boost regulator.

In the factory calibration, the one time programmable[1] digital pot AD5273 is used to adjust various intensity levels. Once the desirable level is determined, a computer program can program such setting permanently and the system can be shipped to the field.

When the system is powered up, we may assume the white LED remains at off due to the delay. The photocell sensor senses no intensity and therefore provides high output resistance. The comparator -IN node becomes high and outputs low if this level is higher than the +IN reference level and makes the up/down control digital pot select to the count down direction. AD5227 will decrement at every clock pulse generated by the clock generator U4, R3, and C1. The continued lowering of P1's gate voltage makes it turn on harder to drive the white LED. The operation reverses when the white LED intensity is higher than the reference level. This system is therefore self-regulated. Although the resolution is limited to ±1.6%, this system is a simple self-contained close loop control and is adaptive if U1 is made adjustable at the field

Constant Bias To Retain Resistance Setting

For users who consider EEMEM pots but cannot justify the additional cost for their designs, they may consider AD5227 as low cost alternatives. They may constantly bias the AD5227 with the supply to retain the resistance setting. AD5227 is designed specifically with low power in mind that allows power conservation even in the battery-operated systems. As shown in Figure 16, a similar low power digital pot is applied in a 3.4V 450mAhour Li-ion cellphone battery. The measurement shows that the device drains negligible power. Constantly bias the pot is not an impractical approach because most of the portable devices nowadays do not require detachable batteries for charging purpose. Although the resistance setting of AD5227 will be lost when the battery needs replacement, such event occurs infrequently that such inconvenience is justified for most applications. And when it happens, user should be provided with a mean to adjust the setting accordingly.

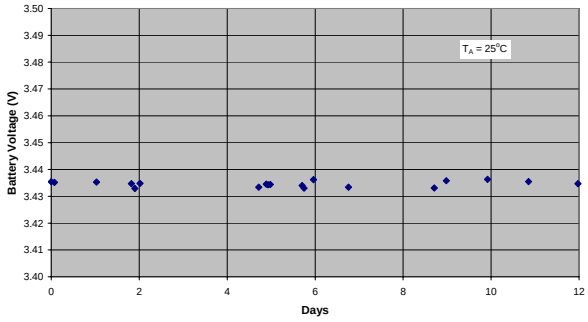

Figure 16. Battery Consumption Measurement.

Outline Dimensions

Dimensions shown in inches and (mm)

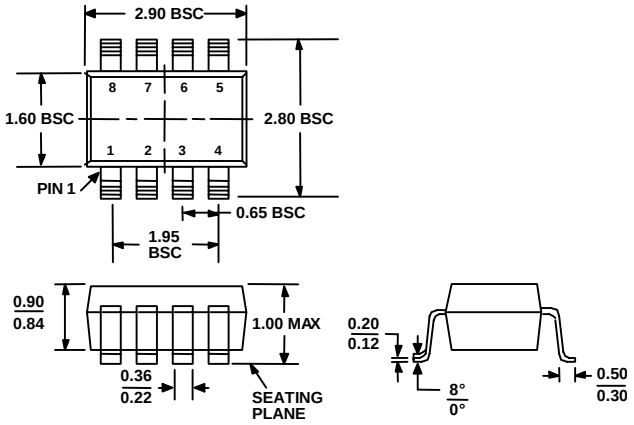

Figure 17. 8-Lead Small Outline Transistor Package [Thin SOT-23] (UJ-8)
Dimensions shown in millimeters

ESD Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 1. Ordering Guide

Model[1]	R_{AB} (kΩ)	Temp Range	Package Code	Package Description	Full Container Quantity	Brand
AD5227BUJZ10-R7	10	-40°C to +105°C	UJ	SOT23-8	3000	D3G
AD5227BUJZ10	10	-40°C to +105°C	UJ	SOT23-8	250	D3G
AD5227BUJZ50-R7	50	-40°C to +105°C	UJ	SOT23-8	3000	D3H
AD5227BUJZ50	50	-40°C to +105°C	UJ	SOT23-8	250	D3H
AD5227BUJZ100-R7	100	-40°C to +105°C	UJ	SOT23-8	3000	D3J
AD5227BUJZ100	100	-40°C to +105°C	UJ	SOT23-8	250	D3J
AD5227EVAL	10				1	

1. Z=Pb Free Parts

The end-to-end resistance RAB is available in 10kΩ, 50kΩ, and 100kΩ. The final three characters of the part number determine the nominal resistance value, e.g., 10kΩ =10.